

DATA SHEET

74HC3G04; 74HCT3G04 Inverter

Product specification

2002 Jul 26

Inverter

74HC3G04; 74HCT3G04

FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Very small 8 pins package
- Output capability: standard.

DESCRIPTION

The 74HC3G/HCT3G04 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). Specified in compliance with JEDEC standard no. 7.

The 74HC3G/HCT3G04 provides three inverting buffers.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f \leq 6.0\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC3G04	HCT3G04	
t_{PHL}/t_{PLH}	propagation delay nA to nY	$C_L = 50\text{ pF}$; $V_{CC} = 4.5\text{ V}$	8	10	ns
C_I	input capacitance		1.5	1.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	9	9	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total switching outputs;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

2. For HC3G the condition is $V_I = \text{GND to } V_{CC}$.
For HCT3G the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$.

FUNCTION TABLE

See note 1.

INPUT		OUTPUT	
nA	nY	nA	nY
L		H	
H		L	

Note

1. H = HIGH voltage level;
L = LOW voltage level.

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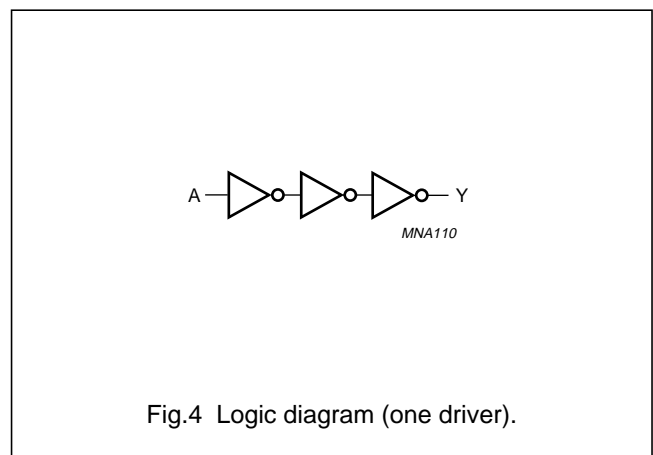
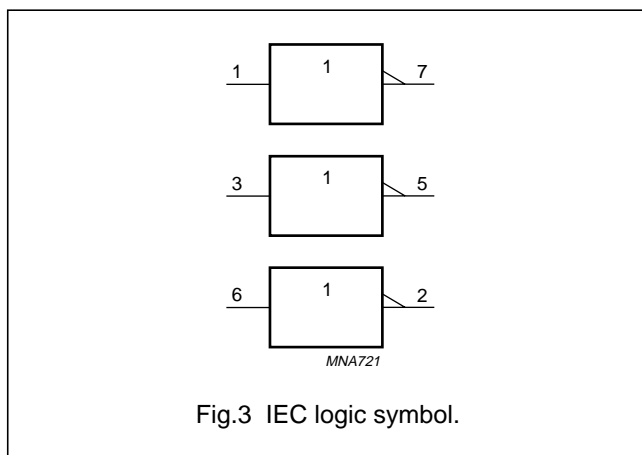
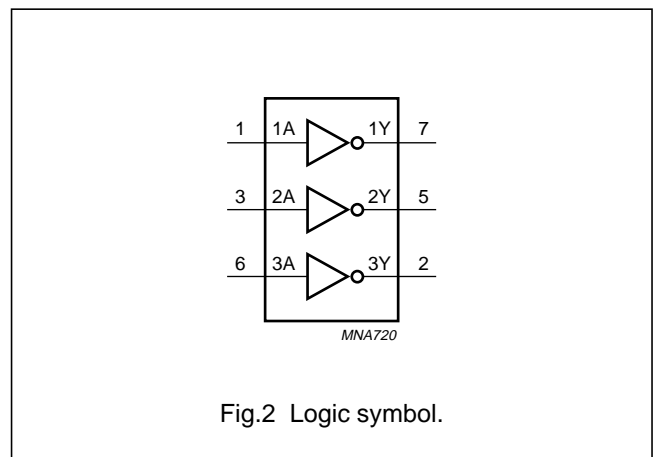
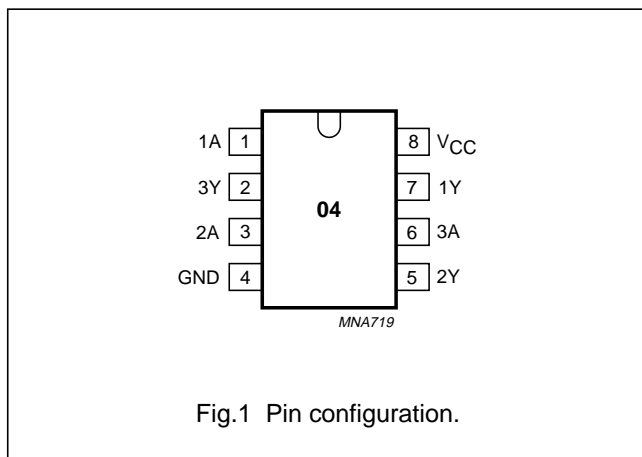
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ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC3G04DP	-40 to +125 °C	8	TSSOP-8	plastic	SOT505-2	H04
74HCT3G04DP	-40 to +125 °C	8	TSSOP-8	plastic	SOT505-2	T04

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input 1A
2	3Y	data output 3Y
3	2A	data input 2A
4	GND	ground (0 V)
5	2Y	data output 2Y
6	3A	data input 3A
7	1Y	data output 1Y
8	V _{CC}	supply voltage



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC3G04			74HCT3G04			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 2.0$ V	–	–	1000	–	–	–	ns
		$V_{CC} = 4.5$ V	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0$ V	–	–	400	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V; note 1	–	±20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1	–	±20	mA
I_O	output source or sink current	-0.5 V < $V_O < V_{CC} + 0.5$ V; note 1	–	25	mA
I_{CC}	V_{CC} or GND current	note 1	–	50	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range from –40 to +125 °C; note 2	–	300	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 110 °C the value of P_D derates linearly with 8 mW/K.

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DC CHARACTERISTICS

Type 74HC3G04

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)						UNIT	
		OTHER	V _{CC} (V)	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
V _{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	1.5	–	1.5	–	V
			4.5	3.15	2.4	–	3.15	–	3.15	–	V
			6.0	4.2	3.2	–	4.2	–	4.2	–	V
V _{IL}	LOW-level input voltage		2.0	–	0.8	0.5	–	0.5	–	0.5	V
			4.5	–	2.1	1.35	–	1.35	–	1.35	V
			6.0	–	2.8	1.8	–	1.8	–	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = –20 µA	2.0	1.9	2.0	–	1.9	–	1.9	–	V
		V _I = V _{IH} or V _{IL} ; I _O = –20 µA	4.5	4.4	4.5	–	4.4	–	4.4	–	V
		V _I = V _{IH} or V _{IL} ; I _O = –20 µA	6.0	5.9	6.0	–	5.9	–	5.9	–	V
		V _I = V _{IH} or V _{IL} ; I _O = –4.0 mA	4.5	4.18	4.32	–	4.13	–	3.7	–	V
		V _I = V _{IH} or V _{IL} ; I _O = –5.2 mA	6.0	5.68	5.81	–	5.63	–	5.2	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = 20 µA	2.0	–	0	0.1	–	0.1	–	0.1	V
		V _I = V _{IH} or V _{IL} ; I _O = 20 µA	4.5	–	0	0.1	–	0.1	–	0.1	V
		V _I = V _{IH} or V _{IL} ; I _O = 20 µA	6.0	–	0	0.1	–	0.1	–	0.1	V
		V _I = V _{IH} or V _{IL} ; I _O = 4.0 mA	4.5	–	0.15	0.26	–	0.33	–	0.4	V
		V _I = V _{IH} or V _{IL} ; I _O = 5.2 mA	6.0	–	0.16	0.26	–	0.33	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	–	–	±0.1	–	±1.0	–	±1.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	1.0	–	10	–	20	µA

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Type 74HCT3G04

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)						UNIT	
		OTHER	V _{CC} (V)	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	2.0	–	2.0	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	–	0.8	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = –20 µA	4.5	4.4	4.5	–	4.4	–	4.4	–	V
		V _I = V _{IH} or V _{IL} ; I _O = –4.0 mA	4.5	4.18	4.32	–	4.13	–	3.7	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = 20 µA	4.5	–	0	0.1	–	0.1	–	0.1	V
		V _I = V _{IH} or V _{IL} ; I _O = 4.0 mA	4.5	–	0.15	0.26	–	0.33	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±0.1	–	±1.0	–	±1.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	1.0	–	10	–	20	µA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} – 2.1 V; I _O = 0	4.5 to 5.5	–	–	300	–	375	–	410	µA

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AC CHARACTERISTICS

Type 74HC3G04

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)						UNIT	
		WAVEFORMS	V _{CC} (V)	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 6	2.0	–	22	75	–	90	–	110	ns
			4.5	–	8	15	–	18	–	22	ns
			6.0	–	6	13	–	16	–	20	ns
t _{THL} /t _{TLH}	output transition time	see Figs 5 and 6	2.0	–	18	75	–	95	–	125	ns
			4.5	–	6	15	–	19	–	25	ns
			6.0	–	5	13	–	16	–	20	ns

Type 74HCT3G04

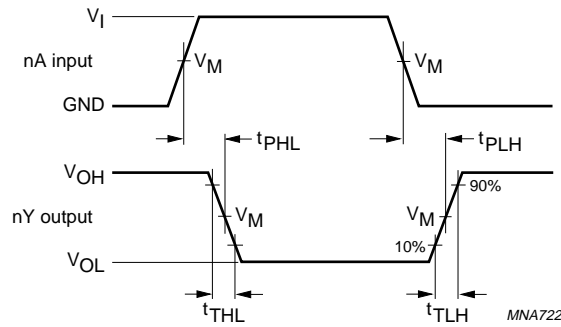
GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)						UNIT	
		WAVEFORMS	V _{CC} (V)	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 6	4.5	–	10	18	–	23	–	29	ns
t _{THL} /t _{TLH}	output transition time	see Figs 5 and 6	4.5	–	6	15	–	19	–	22	ns

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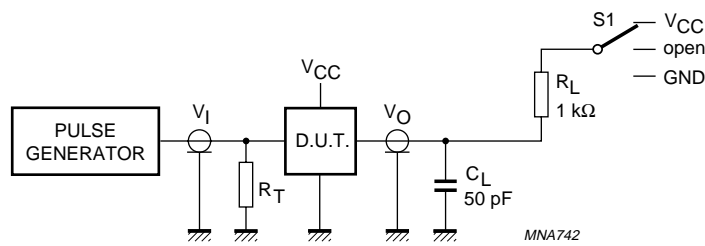
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AC WAVEFORMS



For HC3G: $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 For HCT3G: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3.0 \text{ V}$.

Fig.5 The input (nA) to output (nY) propagation delays and the output transition times.



TEST	S ₁
t _{PLH} /t _{PHL}	open
t _{PLZ} /t _{PZL}	V _{CC}
t _{PHZ} /t _{PZH}	GND

Definitions for test circuit:
 C_L = load capacitance including jig and probe capacitance.
 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

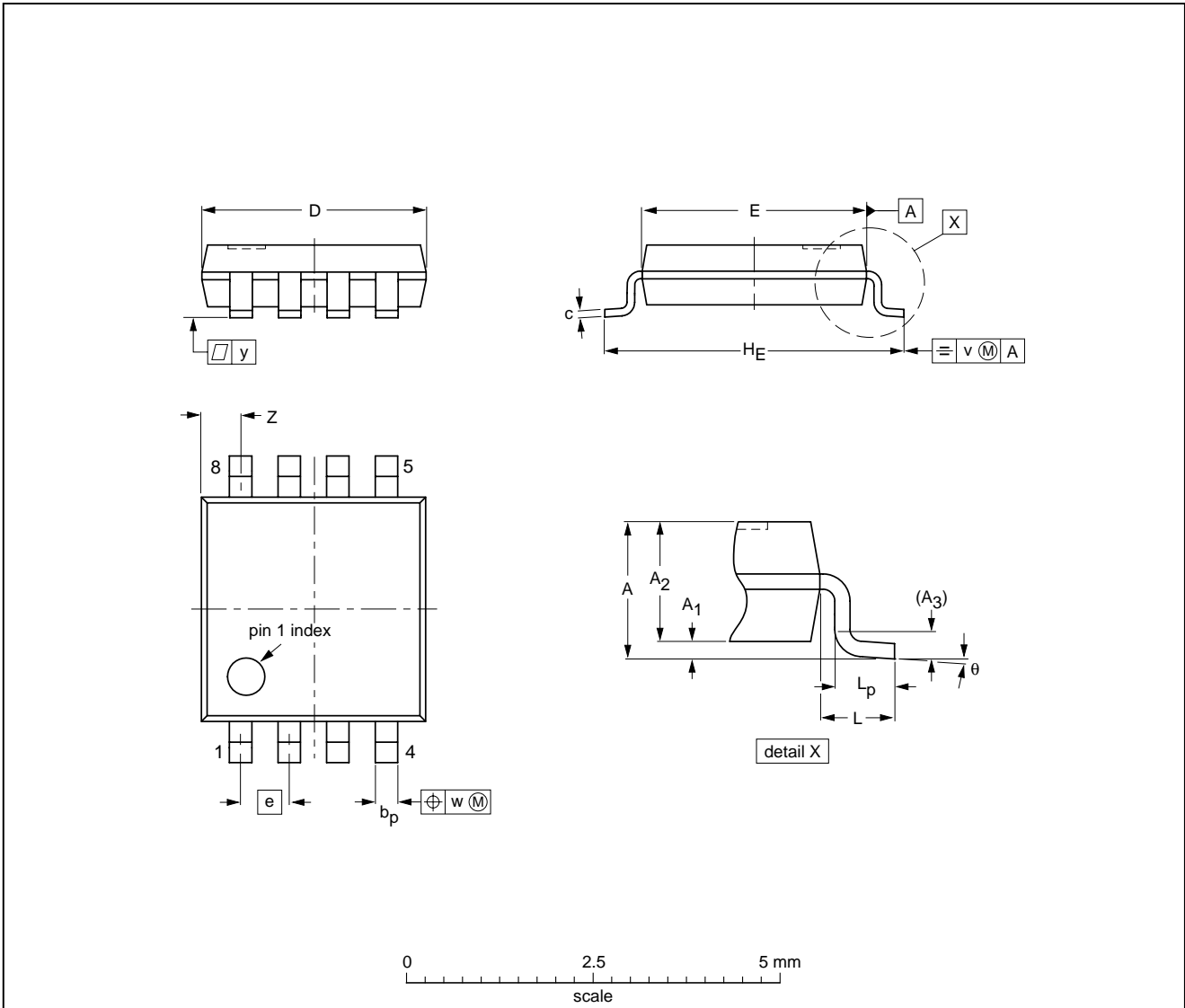
Fig.6 Load circuitry for switching times.

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PACKAGE OUTLINE

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE ⁽¹⁾	SOLDERING METHOD	
	WAVE	REFLOW ⁽²⁾
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ⁽³⁾	suitable
PLCC ⁽⁴⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽⁴⁾⁽⁵⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁶⁾	suitable

Notes

1. For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

DEFINITIONS

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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